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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

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VICARY, KEITH E	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/552,076
Filing Date: October 04, 2005
Appellant(s): TERECHKO, ANDREI

William S. Francos
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/6/2007 appealing from the Office action mailed 4/6/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

The first and second grounds of rejection are no longer to be reviewed on appeal. See below.

Appellant's brief presents arguments relating to the title of the invention, which is the first ground of rejection. This issue relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 1201.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

The second ground of rejection is withdrawn by the examiner.

Therefore, the third and fourth grounds of rejection are to be reviewed on appeal.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6269437	Batten	7-2001
5598408	Nickolls	1-1997
5659785	Pechanek	8-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US 5598408).

Consider claim 1, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, also in col. 7, lines 4-7, clustered processor), comprising a plurality of clusters each comprising at least one register file and at least one functional unit (Figure 12 shows clusters 108, which in col. 11, lines 7-8, show to contain ALUs, also col. 1, lines 43-45, execution units, register file; register files also in col. 3, lines 32-35); an instruction unit (IFD) for issuing control signals to said clusters (Figure 12, fetch and decode units 104 and 106, also col. 11, lines 3-4, fetch and decode unit; the control signals are inherent in D-H of Figure 12 and col. 11, line 65, instruction path), wherein said instruction unit is connected to each of said clusters via respective control connections (D-H of Figure 12 and col. 11, line 65, instruction path), and said pipeline registers being adapted to provide a dedicated direct signal connection between any two of said clusters (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced

connectivity, requiring additional move instructions; col. 3, line 23-43 go into detail about the arrangement).

However, Batten does not disclose that one or more additional pipeline registers is arranged in said control connections depending on the distance between said instruction unit and said clusters.

On the other hand, Nickolls does disclose of one or more additional pipeline registers arranged in control connections depending on the distance between an instruction unit and clusters (col. 6, lines 1-45, pipeline registers; col. 21, lines 13-32 and col. 22, lines 30-42 and 56-62 shows the operation of the pipeline registers; col. 23, lines 13-16, shows multiple pipeline registers per path can be placed for time reasons; col. 59, lines 64-67, col. 60, lines 1-6, allow for different embodiments).

The teaching of Nickolls' of adding in pipeline registers to serve as intermediate points for signals allows for more flexibility in component density, allows for instruction synchronization, allows for greater overall improvements in performance by adding additional clusters/processors, and increases throughput of said signals (Nickolls, stated across col. 2, lines 30-36; col. 2, lines 54-57; col. 2, lines 60-64; col. 3, lines 55-64; col. 4, lines 1-14; col. 5, lines 51-64; col. 20, lines 11-31; col. 23, lines 13-16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals. Furthermore, it

would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls fits into the environment of Batten as both are sending message bits/signals to destination processors/clusters. It would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls also works indiscriminate of whether control signals or data signals are passing through it.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the pipeline registers of Nickolls with the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals.

2. Consider claim 5, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, also in col. 7, lines 4-7, clustered processor), comprising a plurality of clusters each comprising at least one register file and at least one functional unit (Figure 12 shows clusters 108, which in col. 11, lines 7-8, show to contain ALUs, also col. 1, lines 43-45, execution units, register file; register files also in col. 3, lines 32-35); an instruction unit (IFD) for issuing control signals to said clusters (Figure 12, fetch and decode units 104 and 106, also col. 11, lines 3-4, fetch and decode unit; the control signals are inherent in D-H of Figure 12 and col. 11, line 65, instruction path), wherein said instruction unit is connected to each of said clusters via respective control connections (D-H of Figure 12 and col. 11, line 65, instruction path),

and said pipeline registers being adapted to provide a dedicated direct signal connection between any two of said clusters (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced connectivity, requiring additional move instructions; col. 3, line 23-43 go into detail about the arrangement).

However, Batten does not disclose that one or more additional pipeline register is arranged in said control connections depending on the distance between said instruction unit and said clusters.

On the other hand, Nickolls does disclose of one or more additional pipeline registers arranged in control connections depending on the distance between an instruction unit and clusters (col. 6, lines 1-45, pipeline registers; col. 21, lines 13-32 and col. 22, lines 30-42 and 56-62 shows the operation of the pipeline registers; col. 23, lines 13-16, shows multiple pipeline registers per path can be placed for time reasons; col. 59, lines 64-67, col. 60, lines 1-6, allow for different embodiments).

The teaching of Nickolls' of adding in pipeline registers to serve as intermediate points for signals allows for more flexibility in component density, allows for instruction synchronization, allows for greater overall improvements in performance by adding additional clusters/processors, and increases throughput of said signals (Nickolls, stated across col. 2, lines 30-36; col. 2, lines 54-57; col. 2, lines 60-64; col. 3, lines 55-64; col. 4, lines 1-14; col. 5, lines 51-64; col. 20, lines 11-31; col. 23, lines 13-16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals. Furthermore, it would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls fits into the environment of Batten as both are sending message bits/signals to destination processors/clusters. It would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls also works indiscriminate of whether control signals or data signals are passing through it.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the pipeline registers of Nickolls with the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals.

3. Consider claims 2 and 6, Batten discloses said clusters are connected to each other via a point-to-point connection (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced connectivity,

requiring additional move instructions; note that a fully connected structure is a type of point-to-point connection structure).

4. Consider claims 3 and 7, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

5. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claims 3 and 7 above, and further in view of Pechanek et al. (Pechanek) (US 5659785).

6. Consider claims 4 and 8, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

On the other hand, Pechanek does disclose that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate). Furthermore, it is noted that the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art.

Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs. Furthermore, it would have been readily recognized to one of ordinary skill in the art at

the time of the invention that the disclosed bus of Pechanek also fits into the environment of Batten and Nickolls as both are related to communication architectures between a control unit and its corresponding clusters/processor elements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

(10) Response to Argument

Appellant's arguments regarding the grounds of rejection that are presented for appeal begins on page 7 of the appeal brief. The crux of their argument that the rejection is improper is found on page 8, in which appellant disagrees that Batten, et al. teaches the limitation "a dedicated direct signal data signal connection between any two of the clusters. More specifically, Appellant claims on the bottom of page 8 of the appeal brief that a review of Figure 12 and column 10, lines 25-26 and lines 31-35 of the Batten reference reveals no dedicated connection between clusters. Appellant further elaborates in the middle of page 9 that he agrees that the degree of access and method of communication between clusters is disclosed, but not the dedicated connection.

However, examiner maintains that the aforementioned citations of Batten do teach "a dedicated direct signal data signal connection between any two of the clusters."

Although, as explained above, appellant appears to be acknowledging that Batten does teach that there exists a direct signal data signal connection between any two of the clusters, examiner reiterates the citation of column 10, lines 25-26 and lines 31-35. Column 10, lines 25-26, discloses of a "fully connected" interconnection

technique, which was very readily known in not only the processor architecture art but also the computer networks art at the time of the invention to mean that any given node in a network (whether of computers in a computer network or processors in a multiprocessing system) is connected to any other given node. Column 10, lines 31-35, was further cited to verify this well-known understanding of what a "fully connected" network implies, due to its disclosure that a reduced connectivity network would require additional move instructions to get data from one cluster (synonymous with a node in this context) to another; this is because a reduced connectivity network (in other words, a non-fully connected network) is composed of at least one node which is not directly connected to at least one other destination node and would thus need to route data to an intermediary node in order to reach that destination node.

Therefore, appellant's main argument is that Batten does not teach that the connection between any two of the clusters is *dedicated*.

However, examiner maintains that Batten does teach that the connection between any two of the clusters is dedicated. Applicant argues that Figure 12 in particular reveals no dedicated connection between clusters; however, examiner believes that Figure 12 taken by itself does teach the above limitation. As can be clearly seen in Figure 12, there are 4 separate clusters and a shared units cluster 108-1 to 108-4 and 110, and each cluster has separate connections to other clusters labeled by the letters. For example, Cluster 1 has a dedicated connection to cluster 2 via connection I. Cluster 3 has a dedicated connection to cluster 4 via connection P. Cluster 1 has a dedicated connection to cluster 4 via connection K. It is also noted that

this figure also clearly shows that there exists a direct connection between any two clusters, in addition to the column 10 citations above.

Although it is apparent that Figure 12 does teach that the connection between any two of the clusters is dedicated, various citations in the specification of Batten validate this viewpoint. These citations were cited in the advisory action before the filing of the appeal brief, but will be reiterated here. Column 13, lines 5-47, verifies that the connections of Figure 12 are dedicated from one cluster to another; for example, col. 13, line 6 validates that the I connection connects cluster 108-1 to cluster 108-2. Column 12, line 54, verifies the preceding citation in the context of Figure 12 overall as it discloses that the specific connections listed in column 13 are only for a "typical cluster"; thus, each cluster has analogous connections to other clusters. Finally, Figure 17 also shows the I though L connections in cluster 1.

Therefore, examiner maintains that claims 1-8 are properly rejected as Batten does teach the requisite limitations.

Furthermore, applicant does not argue the use of the Nickolls reference, which the examiner has used to teach the pipeline registers arranged in the connection between clusters. It is readily recognized that the argued limitation "adapted to provide a dedicated direct signal data signal connection between any two of said clusters" is not positively recited. The pipeline registers of Nickolls are certainly *capable* of providing a dedicated direct signal data signal connection between any two of said clusters; thus, this limitation is taught by Nickolls as well.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Keith Vicary

10/17/2007

Conferees:

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

/Lynne H Browne/
Lynne H. Browne
Appeal Practice Specialist, TQAS
Technology Center 2100